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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/466,180	12/17/1999	DONALD F. CAMERON	219.373373X0	9860

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Kenyon & Kenyon
1500 K street, N.W.
Suite 700
Washington, DC 20005-1257

EXAMINER	
TRAN, DENISE	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/466,180	Applicant(s) CAMERON ET AL.	
	Examiner Denise Tran	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2003 and 05 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-12 and 14-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3,4,6-12,14 and 15* is/are allowed.

6)☒ Claim(s) *16-18,21-23 and 26-29* is/are rejected.

7)☒ Claim(s) *19,20,24,25,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAIL ACTION

1. The request filed on 5/12/03 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/466180 is acceptable and a CPA has been established. An action on the CPA follows.

2. 1, 3-4, 6-12, and 14-30 are presented for examination. Claims 2, 5, and 13 have been canceled.

3. Claims 1, 3-4, 6-12, and 14-15 are allowable over the prior art of record.

4. Claims 19-20, 24-25, and 29-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horstmann et al., U.S. Patent No. 6,125,433, (hereinafter Horstmann), in view of Watkins, U.S. Patent No. 5,937,436.

As per claim 16, Horstmann shows the invention substantially as claimed, an apparatus, comprising: a storage device which stores translation table entries for virtual to physical address translations (e.g., col. 3, lines 54-60), and a mechanism which flushes individual translation table entry stored in the storage device in accordance with a corresponding translation cacheable flag (i.e., valid bit) (e.g. col. 4, lines 30-34, col. 11, lines 25-35) included in the individual translation table entry (e.g., fig. 6, VB=0; col. 7, lines 6-8; col. 11, lines 34-36).

Horstmann does not explicitly show the use of protection in the translation table entries. Watkins (e.g., col. 4, lines 41-45; col. 7, lines 55-64) shows the use of protection translation table entries. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have protection bits of Watkins into the translation table entries of Horstmann because it would provide protection of read only memory pages, thereby increasing data security from unwanted writing.

As per claim 17, Horstmann shows wherein the storage device corresponds to an internal cache for storing the translation table entries (e.g., col. 3, lines 54-60). Horstmann does not explicitly show the use of protection in the translation table entries. Watkins (e.g., col. 4, lines 41-45; col. 7, lines 55-64) shows the use of protection translation table entries. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have protection bits of Watkins into the translation

table entries of Horstmann because it would provide protection of read only memory pages, thereby increasing data security from unwanted writing.

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horstmann et al., U.S. Patent No. 6,125,433, (hereinafter Horstmann), in view of Watkins, U.S. Patent No. 5,937,436; and further in view of Futral, U.S. Patent No. 6,112,263.

As per claim 18, Horstmann shows wherein each of the translation table entries represents translation of a single page of a memory (e.g., col. 1, lines 56-60; col. 2, lines 8-14; col. 3, lines 65-67). Horstmann does not explicitly show the use of protection in the translation table entries and a host memory. Watkins (e.g., col. 4, lines 41-45; col. 7, lines 55-64) shows the use of protection translation table entries and a workstation (e.g. figure 2A, element 200) comprising a main memory (e.g. figure 2A, element 220), a workstation fabric adapter (e.g. figure 2A, element 260k). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Watkins into the system of Horstmann because it would provide protection of read only memory pages, thereby increasing data security from unwanted writing. Watkins and Horstmann do not explicitly show the use of a host memory. Futral shows the use of a host comprising a host memory (e.g. col. 1, lines 37- 45; col. 7, lines 47- 55; figure 2a, el. 212 comprising el. 230). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral with Watkins and Horstmann because it would provide a main computer having

a memory storing its data in a system connected by a communication link; and provide many concurrent processes running within the system to be controlled and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28).

8. Claims 21-23, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (5,937,436), in view of Horstmann et al., U.S. Patent No. 6,125,433, (hereinafter Horstmann), and further in view of Futral, U.S. Patent No. 6,112, 263.

As per claims 26 and 21, Watkins shows the use of the adapter (e.g., fig. 2A, element 260K) in a system provided to interface a switched fabric (e.g., fig. 3, an ATM Switch and network; col. 3, lines 14-18), comprising: a cache memory (i.e., a memory in which frequently used data values being duplicated for quick access) for storing a set of translation and protection table entries from the memory (e.g., figure 4, element 450 and col. 2, lines 14-22; col. 1, lines 54-68; col. 6, lines 3-14; col. 6, lines 49-65 and col. 7, lines 60-65) for virtual to physical address translations and access validation to the memory during I/O (e.g. col. 2, lines 14-22 and col. 6, lines 43-65 and figure 5, col. 7, line 5, lines 59-63 and col.1, lines 64-68), each of the TPT entries corresponds to a memory portion of the memory (e.g. col. 2, lines 14-22 and col.1, lines 64-68; col. 3, lines 28-33 and col. 6, lines 55-60) and comprises at least a translation cacheable flag (e.g., col. 6, lines 5-45; col. 8, lines 24-45); and a mechanism to determine a status of the translation cacheable flag of one or more selected TPT entries stored in the cache of the adapter (e.g., col. 6, lines 5-45; col. 8, lines 24-45). Watkins does not explicitly

show discarding the one or more selected TPT entries from the cache based on the status of the translation cacheable flag or checking a status of the translation cacheable flag to determine whether to discard one or more selected TPT entries from the cache of the adapter. Horstmann shows the use of discarding the one or more selected table entries from the cache based on the status of the translation cacheable flag or using a status of the translation cacheable flag to determine whether to discard one or more selected table entries from the cache of the adapter (e.g., col. 11, lines 25-35; col. 10, lines 1-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann with Watkins because it would increase translation speed from limiting a number of reloading currently used data, reduced chip area for fabrication, and supports efficient operation as taught by Horstmann, col. 4, lines 43-49. Watkins and Horstmann do not explicitly show the use of host. Futral shows the use of host (e.g. col. 1, lines 37- 45; col. 7, lines 47- 55; figure 2a, el. 212, 230). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and provide many concurrent processes running within the system to be controlled and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28.

As per claims 22 and 27, Watkins teaches the use of the adapter and TPT entry as discussed above. Watkins does not explicitly show the use an operating system to set the status of the translation cacheable flag per TPT entry for enabling to discard

individual TPT entries from the cache. Horstmann shows the use of an operating system to set the status of the translation cacheable flag per table entry for enabling to discard individual table entries from the cache (e.g. col. 11, lines 25; col. 1, lines 17-19 and col. 1, lines 49-55; col. 10, lines 1-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Horstmann into the system of Watkins because it would increase translation speed from limiting number of reloading currently used data, reduce chip area for fabrication, and supports efficient operation as taught by Horstmann, col. 4, lines 43-49.

As per claims 23 and 28, Watkins shows the use of each of the selected translation and protection table entries represents translation of a single page of the main memory (e.g. col. 3, lines 28-33 and col. 6, lines 55-60). Watkins and Horstmann do not explicitly show the use of host. Futral shows the use of host (e.g. col. 1, lines 37-45; col. 7, lines 47- 55; figure 2a, el. 212, 230). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Futral with Watkins and Horstmann because it would provide a main computer in a system connected by a communication link; and provide many concurrent processes running within the system to be controlled and a secure manner as taught by Futral col. 2, lines 49-51 and col. 2, lines 25-28.

9. Applicant's arguments filed 3/13/03 have been fully considered but they are not persuasive.

10. In the remarks, the applicant argued that Horstmann did not teach the corresponding translation cacheable flag **included in** translation and protection table (TPT) entries.

The examiner disagreed with the applicant arguments because Horstmann teaches the corresponding translation cacheable flag (I.e., valid bit) **included in** the individual translation table entry. As the applicant admitted that Horstmann shown "the **valid bit included in the slice** is set ," the applicant amendment after final filed 03/13/03, page 8, lines 9-10.

Also, Horstmann shows the corresponding translation cacheable flag **included** in or **a part of** the individual translation table entry, such as col. 7, line 16, "the valid bit **of** each slice"; fig. 6, **slice C included VB=0** wherein at the initial operation **all the entries (i.e., slices) included their VB=0,** col. 7, lines 20-30; fig. 11B, a valid bit **included in** the LRU 60 within a slice of the TLB; and col. 8, lines 45-47, "each slice **having** its associated valid bit set."

In further discussion, the combination of Horstmann and Watkins, not individually, teaches the use of a corresponding translation cacheable flag included in an individual translation and protection table (TPT) entry as recited in the rejections above. In particular, Horstmann teaches the use of a corresponding translation cacheable flag **included in** an individual translation table entry (e.g., fig. 6, VB=0; col. 7, lines 6-8; col. 11, lines 34-36. Horstmann does not explicitly show the use of protection in the translation table entries. Watkins (e.g., col. 4, lines 41-45; col. 7, lines 55-64) shows the use of protection translation table entries. It would have been obvious

to one of ordinary skill in the art at the time the invention was made to have protection bits of Watkins into the translation table entries of Horstmann because it would provide protection of read only memory pages, thereby increasing data security from unwanted writing.

11. In the remarks, the applicant argued that the citation was misplace because fig. 6 of Horstmann show a slice or row of the adjacent CAM, RAM and LRU columns as shown in fig. 5 but did not shows the corresponding translation cacheable flag (i.e., valid bit) **included in** the individual translation table entry .

In response to the applicant's argument that the citation is not misplace because the citation clearly shows the corresponding translation cacheable flag **included in** the individual translation table entry, Horstmann, fig. 6, VB=0 is **included in** the slice C wherein the slice C is an entry of the translation table as recited in col. 7, lines 6-8.

12. In the remarks, the applicant argued that Horstmann does not disclose the use of **flushing the individual TPT entry in accordance with the corresponding translation cacheable flag**.

In response to the applicant's argument that the combination of Horstmann and Watkins, not individually, teaches the use of flushing the individual TPT entry in accordance with the corresponding translation cacheable flag as recited in the rejections above. In particular, Horstmann teaches the use of a corresponding

translation cacheable flag included in an individual translation table entry (e.g., fig. 6, VB=0; col. 7, lines 6-8; col. 11, lines 34-36) in order **to flush the individual table entry in accordance with the corresponding translation cacheable flag (e.g. col. 11, lines 25-35; col. 4, lines 30-34)**. According to col. 11, lines 25-35, Horstmann teaches flushing the individual translation entry by comparing the requested virtual address **in accordance with each valid entry having its corresponding translation cacheable flag set** (i.e., valid bit status set) within the CAM but not an invalid entry which having its corresponding translation cacheable flag reset. Also, Horstmann, col. 11, lines 25-35, teaches flushing the individual translation **entry in accordance with the corresponding translation cacheable flag of that entry being reset**. Horstmann does not explicitly show the use of protection in the translation table entries. Watkins (e.g., col. 4, lines 41-45; col. 7, lines 55-64) shows the use of protection translation table entries. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have protection bits of Watkins into the translation table entries of Horstmann because it would provide protection of read only memory pages, thereby increasing data security from unwanted writing.

13. In the remark, the applicant argued that Watkins did not suggest the use of a translation cacheable flag included in each TPT entry.

The examiner disagreed with the applicant's arguments because Watkins also teaches a translation cacheable flag (i.e., valid bit) included in each TPT entry (e.g., col. 6, lines 3-45).

14. In the remarks, the applicant argued that there is no teaching or suggestion in the prior art to arrive at the applicant's claimed invention.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Horstmann shows the invention substantially as claimed, an apparatus, comprising: a storage device which stores translation table entries for virtual to physical address translations (e.g., col. 3, lines 54-60), and a mechanism which **flushes individual translation table entry stored in the storage device in accordance with a corresponding translation cacheable flag (i.e., valid bit) (e.g. col. 4, lines 30-34, col. 11, lines 25-35) included in the individual translation table entry (e.g., fig. 6, VB=0; col. 7, lines 6-8; col. 11, lines 34-36)**.

Horstmann does not explicitly show the use of protection in the translation table entries. Watkins (e.g., col. 4, lines 41-45; col. 7, lines 55-64) shows the use of protection translation table entries. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have protection bits of Watkins into the

translation table entries of Horstmann because it would provide protection of read only memory pages, thereby increasing data security from unwanted writing.

15. In the remarks, the applicant's argued that the examiner has incorrectly interpreted the teachings of Horstmann, failed to considered all the limitations of claims 16-17, and fail to provide any suggestion or motivation to modify Watkins into Horstmann in order to arrive the applicant's claims 16-17.

In response to the applicant's argument, the examiner has correctly interpreted the teachings of Horstmann, considered all the limitations of claims 16-17, and provided the suggestion or motivation to modify Watkins into Horstmann in order to arrive the applicant's claims 16-17, as stated in the rejections and the examiner's responses to the applicant's arguments above.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday, and an alternate Wed. from 8:30 a.m. to 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7467-239 for Official communications, (703) 746-7240 for Non Official communications, and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

D.T.
July 18, 2003